SNJB's

Late Sau. Kantabai Bhavarlalji Jain

College of Engineering

(An Autonomous Institute Affiliated to Savitribai Phule Pune University, Pune)

Shri Neminath Jain Brahmacharyashram (SNJB) (Jain Gurukul)

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ESTD - 1928

Curriculum and Evaluation Scheme for Second Year B. Tech. in

Electronics & Telecommunication Engineering with Multidisciplinary Minor and Honor

CHAIRMAN
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LSKBJ COLLEGE OF ENGINEERING
Chandwad Dist.Nashik

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Chandwad
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Pin-423101

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ACADEMIC COUCIL
SNJB's
LSKBJ COLLEGE OF ENGINEERING
Chandwad Dist.Nashik

To be implemented for 2024-28 Batch
(With Effect from Academic Year 2025-26)

Vision of the Institute

Transform young aspirant learners towards creativity and professionalism for societal growth through quality technical education.

Mission of the Institute

1. To transfer the suitable technology, particularly for rural development.
2. To enhance diverse career opportunities among students for building a nation.
3. To acquire the environment of learning to bridge the gap between industry and academics.
4. To share values, ideas, and beliefs by encouraging faculties and students for the welfare of society.

Vision of the Electronics & Telecommunication Engineering Department

To prepare Electronics & Telecommunication Engineers for the benefit of the society.

Mission of the Electronics & Telecommunication Engineering Department

1. To provide quality education to students
2. To enrich the skill in collaboration with industry for better career opportunity
3. To inculcate ethics, values and environment awareness

Program Outcomes (POs) for an engineering graduate:

PO1: Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)

PO3: Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)

PO4: Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions. (WK8).

PO5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)

PO6: The Engineer and The World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, and WK7).

PO7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)

PO8: Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.

PO9: Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences

PO10: Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO11: Life-Long Learning: Recognize the need for, and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

Program Specific Outcomes

1. PSO1: Apply their skills in designing, implementing and testing electronic systems.
2. PSO2: Demonstrate proficiency in use of modern electronic design automation (EDA) tools.
3. PSO3: Communicate and work effectively as individuals and as team members.

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Curriculum and Evaluation Scheme for Second Year B. Tech. in Electronics & Telecommunication Engineering with Multidisciplinary Minor

To be implemented for 2024-28 Batch

(With Effect from Academic Year 2025-26)

GENERAL COURSE STRUCTURE

A. Definition of Credit:

Table 1: Credit Definition

1 Hour Lecture (L) per week	1 Credit
1 Hour Tutorial (T) per week	1 Credit
2 Hours Practical (P) per week	1 Credit

B. Range of Credits: (B.Tech. or Equivalent) in Tech. with Multidisciplinary Minor:

In the light of the fact that a typical NEP Compliant Model Four-year Undergraduate degree program in Technology has about 176 credits, the total number of credits proposed for the four-year B.Tech. in **Electronics & Telecommunication Engineering** with Multidisciplinary minor degree is kept as **172.**

Table 2: Range of Credits

Course Category		Credits As PER NEP Guidelines	Proposed Credits
Basic Science Course	BSC/ESC	14-18	15
Engineering Science Course		16-12	14
Programme Core Course (PCC)	Program Courses	44-56	47
Programme Elective Course (PEC)		20	20
Multidisciplinary Minor (MD M)	Multidisciplinary Courses	14	17
Open Elective (OE) Other than a particular program		8	8
Vocational and Skill Enhancement Course (VSEC)	Skill Courses	8	8
Ability Enhancement Course (AEC)	Humanities Social Science and Management (HSSM)	4	6
Entrepreneurship/Economics/ Management Courses		2	4
Indian Knowledge System (IKS)		2	2
Value Education Course (VEC)		4	5
Research Methodology(RM)	Experiential Learning Courses	4	4
Community Engagement Project (CEP)/ Field Project (FP)		2	2
Project		4	5
Internship/ OJT		12	12
Co-curricular Courses (CC)	Liberal Learning Courses	4	3
Total Credits		**160-176**	**172**

C. Semester wise Credit Distribution Structure for Four Year B. Tech in Electronics & Telecommunication Engineering Engineering with Multidisciplinary Minor:

Table3: Semester-wise Credit Distribution Structure

Semester		I	II	III	IV	V	VI	VII	VIII	Total Credits
Basic Science Course	BSC/ESC	8	7	-	-	-	-	-	-	15
Engineering Science Course		7	7	-	-	-	-	-	-	14
Programme Core Course (PCC)	Program Courses	-	3	11	8	9	4	9	3	47
Programme Elective Course (PEC)		-	-	-	-	6	5	6	3	20
Multidisciplinary Minor (MD M)	Multidisciplinary Courses	-	-	3	3	3	2	3	3	17
Open Elective (OE) Other than a particular program		-	-	-	3	2	3	-	-	8
Vocational and Skill Enhancement Course (VSEC)	Skill Courses	2	2	-	2	-	2	-	-	8
Ability Enhancement Course (AEC)	Humanities Social Science and Management (HSSM)	1	-	1	2	2	-	-	-	6
Entrepreneurship/Economics/ Management Courses		-	-	2	2	-	-	-	-	4
Indian Knowledge System (IKS)		2	-	-	-	-	-	-	-	2
Value Education Course (VEC)		-	-	3	2	-	-	-	-	5
Research Methodology	Experiential Learning Courses	-	-	-	-	-	4	-	-	4
Community Engagement Project (CEP)/ Field Project (FP)		-	-	2	-	-	-	-	-	2
Project		-	-	-	-	-	2	3	-	5
Internship / OJT		-	-	-	-	-	-	-	12	12
Co-curricular Courses (CC)	Liberal Learning Courses	1	2	-	-	-	-	-	-	3
Total Credits (Major)		**21**	**21**	**22**	**22**	**22**	**22**	**21**	**21**	**172**

Students can opt for any of the following as per the rules and regulations given by the institute:

1. B. Tech with Multidisciplinary Minor = Total 172 Credits
2. B. Tech with Multidisciplinary Minor and Honor = Total 190 Credits

HONORS

- In addition to 172 credits of B. Tech Programmes (Bachelor of Technology) i.e. Major in which the student has taken admission, a student may opt for Honors in the same Tech. discipline/branch / Emerging Areas.
- A student is required to earn an additional 18 credits in the same Tech. discipline/ branch / Emerging Areas for Honors distributed over semesters III to VIII.
- The total number of credits required to complete the Honors in the same Tech. discipline/ Emerging Areas is 18 credits, in addition to 172 credits in Major.
- Students will have to compulsorily choose Honors from the same Tech. discipline/branch.
- Honors Degree in the Bachelor of Engineering programme shall be awarded to students earning additional total credits of all six semesters from the second year to final year, i.e., 18 Credits, in addition to 172 credits or 130 credits respectively. The student admitted in the first year must earn 172 credits and 130 credits admitted in lateral entry (admitted after Diploma or B.Sc.) in the second year.
- Minor Courses can be completed through an online platform.

The student has to choose One Honor out of the Two Honor groups provided below

Honors offered by Electronics & Telecommunication Engineering are as follows:

Table 4: Honors

Sr No	Name of Honors Offered by Department
A.	VLSI Design
B.	Robotics

The detailed syllabus structure for the same is as follows:

Table 5A: Specialization Honors in VLSI Design

Sr. No	Category	SEM	Course Code	Course Name	Teaching Scheme				
					Hours				Credits
					L	T	P	Total Hours	
01	HOC	III	24-HOC-ET-2-01A	VLSI Technology	3	-	-	3	3
02	HOC	IV	24-HOC-ET-2-02A	VLSI Design Flow	3	-	-	3	3
03	HOC	V	24-HOC-ET-3-03A	VLSI Testing & Testability	3	-	-	3	3
04	HOC	VI	24-HOC-ET-3-04A	VLSI Interconnect	3	-	-	3	3
05	HOC	VII	24-HOC-ET-4-05A	Digital CMOS Design	3	-	-	3	3
06	HOC	VIII	24-HOC-ET-4-06A	Analog CMOS Design	3	-	-	3	3
Total					**18**	-	-	**18**	**18**

Table 5B: Specialization Honors in Robotics

Sr. No	Category	SEM	Course Code	Course Name	Teaching Scheme				
					Hours				Credits
					L	T	P	Total Hours	
01	HOC	III	24-HOC-ET-2-01B	Introduction to Robotics	3	-	-	3	3
02	HOC	IV	24-HOC-ET-2-02B	Fundamental of Power Electronics	3	-	-	3	3
03	HOC	V	24-HOC-ET-3-03B	Robotics: Basics and Selected Advanced Concepts	3	-	-	3	3
04	HOC	VI	24-HOC-ET-3-04B	Wheeled Mobile Robots	3	-	-	3	3
05	HOC	VII	24-HOC-ET-4-05B	Mechanism And Robot Kinematics	3	-	-	3	3
06	HOC	VIII	24-HOC-ET-4-06B	Advanced Robotics	3	-	-	3	3
Total					**18**	-	-	**18**	**18**

#Note for NPTEL/SYAYAM: Approved courses and platforms will be enlisted timely by authorities along with rules and regulations

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Honors Syllabus for SEM III and SEM IV

24-HOC-ET-2-01A: VLSI Technology

Teaching Scheme:	**Credit:** 3	**Examination Scheme:**
Theory: 3 Hours/Week		**CIE** : 20 Marks **MSE :** 20 Marks **SEE** : 60 Marks

Prerequisites Courses: 24-BSC-1-01 : Engineering Physics

Companion Course: -

Course Objectives:

- Introduce Semiconductor Material Preparation & Growth Techniques
- Provide an In-Depth Understanding of Diffusion, Lithography, sEtching & Thin Film Deposition processes
- Explore Microelectronic Device Packaging & Reliability Considerations

Course Outcomes:
After completion of the course, learners should be able to

CONo	Course Outcomes	BL
CO1	**Understand** Semiconductor Material Preparation & Processing	2
CO2	**Learn** Doping, Diffusion & Lithography Techniques	2
CO3	**Understand** Etching & Thin Film Deposition process in VLSI Fabrication	2
CO4	**Demonstrate** Knowledge of Microelectronic Packaging & Reliability	2

Course Contents

Unit I	Crystal growth, wafer preparation & Epitaxy	10 Hours

Crystal growth & wafer preparation, Processing considerations: Chemical cleaning, gettering the thermal stress factors etc. Vapors phase epitaxy basic transport processes & reaction kinetics, doping & auto doping, equipment & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

Case Studies: TSMC's Silicon Wafer & Epitaxy Process for Advanced Node Technology

*Mapping of Course Outcomes	CO1

Unit II	Oxidation	6 Hours

Growth mechanism & kinetics, silicon oxidation model, interface considerations, orientation dependence of oxidation rates in thin oxides, oxidation techniques & systems, dry & wet oxidation, masking properties of SiO2.

Case Studies: Silicon Oxidation & High-K Dielectrics in Intel's 10nm & 7nm Process Nodes

***Mapping of Course Outcomes**	**CO1**	
Unit III	**Diffusion**	**6 Hours**
Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source/an ion implanted layer.		
Case Studies: Intel's Use of Diffusion & Ion Implantation in 10nm & 7nm FinFET Technology.		
***Mapping of Course Outcomes**	**CO2**	
Unit IV	**Lithography**	**7 Hours**
Optical Lithography: optical resists, contact & proximity printing, projection printing, Electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X-ray sources & masks. Ion lithography.		
Case Studies: TSMC's Adoption of EUV Lithography for Advanced Semiconductor Manufacturing		
***Mapping of Course Outcomes**	**CO2**	
Unit V	**Etching**	**7 Hours**
Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive ion beam etching, specific etches processes: poly/polycide. Trench etching.		
Case Studies: TSMC's Use of Reactive Ion Etching (RIE) for Advanced Transistor Fabrication.		
***Mapping of Course Outcomes**	**CO3**	
Unit VI	**Thin Film Materials & their Deposition**	**6 Hours**
Interlayer dielectrics in microelectronic devices, interconnections within and between different electronic devices. Packaging of Microelectronic Devices: Packaging materials, different types of packaging, Microelectronic devices reliability.		
Case Studies: Intel's Foveros for High-Performance Computing (HPC) & AI Chips		
***Mapping of Course Outcomes**	**CO3, CO4**	
Learning Resources		
Text Books		
T1. J. D. Plummer, Michael D. and Peter D. Griffin, Silicon VLSI Technology: Fundaments, Practice and Modelling **T2.** S. K. Gandhi, VLSI Fabrication Principles, Second edition, Wiley India Pvt. Ltd.		
Reference Books :		
R1. S.M. Sze, "VLSI Technology", McGraw Hill, 2nd Edition. 2008		

R2. Chen, VLSI Technology, Wiley, March 2003

MOOC Courses links :

- https://archive.nptel.ac.in/courses/108/101/108101089/

24-HOC-ET-2-02A: VLSI Design Flow

Teaching Scheme:	**Credit:** 3	**Examination Scheme:**
Theory: 3 Hours/Week		**CIE** : 20 Marks **MSE :** 20 Marks **SEE** : 60 Marks

Prerequisites Courses: 24-HOC-ET-2-01A: VLSI Technology

Companion Course: -

Course Objectives:

- To provide students with a comprehensive understanding of the steps, techniques, and tools involved in the design of Very Large Scale Integration (VLSI) Digital circuits.

Course Outcomes:

After completion of the course, learners should be able to

CONo	**CO**	**BL**
CO1	**Explain** the VLSI design flow for digital circuits	**2**
CO2	**Develop** Verilog-based hardware models and simulate digital circuits	**3**
CO3	**Understand** RTL synthesis, logic optimization, and formal verification techniques	**2**
CO4	**Apply** static timing analysis, technology mapping, and power-driven optimizations to improve the performance and power efficiency	**3**

Course Contents

Unit I	**VLSI Design Flow**	**7 Hours**

Introduction to Integrated Circuits: Structure, Photolithography, Designing vs. Fabrication, Types, Economics, Figures of Merit; Realizing an "Idea" using an IC; Pre-RTL Methodologies, RTL to GDS Implementation Flow, Verification Techniques, Testing Techniques, Post-GDS Processes:

Case Studies: Design flow for Fabrication of a High-Performance AI Accelerator Chip.

***Mapping of Course Outcomes**	**CO1**

Unit II	**Hardware Modeling and Simulation Using Verilog**	**7 Hours**

Modeling Hardware using Verilog: Hardware Description Languages**,** Basic Constructs of Verilog; **Simulation**: Simulator, Testbench, Mechanism,

#Exemplar/Case Studies: Verilog-Based Design and Simulation of a RISC-V Processor.

***Mapping of Course Outcomes**	**CO2**	
Unit III	**RTL synthesis & Formal Verification**	**7 Hours**
RTL synthesis: Logic Synthesis Tasks,Parsing, Elaboration, Verilog Constructs to Hardware; condition. **Formal Verification**: Simulation versus Formal Verification, Model Checking (motivation and examples only), Combinational Equivalence Checking (motivation, register matching and examples),		
#Exemplar/Case Studies: RTL Synthesis and Formal Verification of a High-Performance DSP Core		
***Mapping of Course Outcomes**	**CO3**	
Unit IV	**Logic Optimization & Technology Library**	**7 Hours**
Logic Optimization: Two-level Logic Optimization, Multilevel Logic Optimization, and Technology **Library**: Library Characterization, Timing Attributes and Non-Linear Delay Model.		
#Exemplar/Case Studies: Logic Optimization in the Design of a Low-Power AI Inference Engine/Technology Library Development for a 3nm AI Accelerator Chip		
***Mapping of Course Outcomes**	**CO3**	
Unit V	**Static Timing Analysis**	**7 Hours**
Static Timing Analysis: Behavior of Synchronous Circuit, Setup Requirement, Hold Requirement, Data Paths and Clock Paths, Delay Calculation, Arrival Time, Required Time and Slack Computation; **Constraints**: Clock Constraints, IO Constraints, Timing Exception.		
#Exemplar/Case Studies: Static Timing Analysis for a High-Performance 5nm AI Accelerator		
***Mapping of Course Outcomes**	**CO4**	
Unit VI	**Technology Mapping & Power Analysis**	**7 Hours**
Technology Mapping: Structural Mapping, Boolean Mapping**, Timing-driven optimizations**: Transformations **Power Analysis**: Components, Power Models, Computing Power Dissipation, **Power-driven Optimizations:** Strategies, Register Transfer Level Techniques, Logic-level Techniques, Circuit-level Techniques, Clock Gating, Clock Domains.		
#Exemplar/Case Studies: Technology Mapping and Power Optimization in a 5nm Mobile SoC (Smartphone Processor)		
***Mapping of Course Outcomes**	**CO4**	
Learning Resources		
Text Books		
T1. Sneh Saurabh, Introduction to VLSI Design Flow, Cambridge University Press **T2.** Giovanni Micheli, Synthesis & Optimization of Digital Circuits, TMH		

Reference Books :
R1. Prasad K. G, *Static Timing Analysis for Nanometer Designs: A Practical Approach*, Springer. **R2.** Kaushik Roy Sharat Prasad, Low Power CMOS VLSI Circuit Design, Wiley India
Additional Resources: (Books, e-Resources)
MOOC Courses links : ● https://nptel.ac.in/courses/108106191 ● https://nptel.ac.in/courses/108107380

24-HOC-ET-2-01B: Introduction to Robotics

Teaching Scheme:	**Credits:** 3	**Examination Scheme:**
Theory: 3 Hours/Week		**CIE** : 20 Marks **MSE :** 20 Marks **SEE** : 60 Marks

Prerequisite Courses: 24-ESC-1-01 Basic Electrical and Electronics Engineering

Companion Course:

Course Objectives:

- To provide overview of Robotics Technology
- To inculcate the ability to recognize sensors and actuators used in Robotics
- To introduce Robot Kinematics
- To acquire knowledge about Robotics Applications

Course Outcomes:
After completion of the course, learners should be able to

CONo	CO	BL
CO1	**Explicate** the basics of Robotics	**2**
CO2	**Explain** Kinematics and Dynamics in Robotics	**2**
CO3	**Select** motor for robotic application	**4**
CO4	**Explain** Probabilistic Robotics	**2**
CO5	**Select** ight localization techniques for robotic application	**4**

Course Contents

Unit I	**Introduction to robotics**	**7 Hours**

History, growth; Robot applications- industrial robots, field and service robots,, Manufacturing industry, defense, rehabilitation, medical etc., Laws and the ethical considerations surrounding robotics

#Exemplar/Case Studies: Examine the development of robotics from early industrial robots like Unimate to AI-powered collaborative robots (cobots) and autonomous systems.

***Mapping of Course Outcomes**	**CO1**

Unit II	**Robot mechanisms**	**7 Hours**

Kinematics- coordinates transformations, Homogeneous Transformation Matrix, Yaw-Pitch-Roll transformation, concept of

degrees of freedom, holonomic, non-holonomic, and redundant systems based on their controllable degrees of freedom.		
#Exemplar/Case Studies: Examine how Autonomous Mobile Robots (AMRs) operate within constraints for Warehouse application		
***Mapping of Course Outcomes**	**CO2**	
Unit III	**Robot Architecture and Kinematics**	**7 Hours**
Robot Architectures, Kinematic Parameters, DH Algorithm, Forward Kinematics, Inverse Kinematics, Differential Relations, Manipulator Jacobian & Statics .		
#Exemplar/Case Studies: Discuss how inverse kinematics algorithms enable to achieve human-like motion, balance, and agility		
***Mapping of Course Outcomes**	**CO2**	
Unit IV	**Actuators in Robotics**	**7 Hours**
Overview & Operational needs of Electric Actuators, Principles of DC Motor Operation, DC Motor Control Regions, H-Bridge DC Motor Control Structure, Brushless DC Machine, Control of the Brushless DC Motor, PM Synchronous Motor, Encoders for Speed & Position Estimation, Stepper Motors		
#Exemplar/Case Studies: DC Motor Speed Control in Industrial Conveyor System		
***Mapping of Course Outcomes**	**CO3**	
Unit V	**Probabilistic Robotics**	**7 Hours**
Introduction to Probabilistic Robotics, Recursive State Estimation: Bayes Filter, Probability Basics, Kalman Filter, Velocity Motion Model , Rangefinder Measurement Model		
#Exemplar/Case Studies: Autonomous Navigation in Self-Driving Cars		
***Mapping of Course Outcomes**	**CO4**	
Unit VI	**Localization**	**7 Hours**
Global and local localization, passive versus active approaches, challenges of dynamic environments, selecting the right localization techniques for robotic application, Markov localization, fundamental path planning algorithms. breadth-first search, Dijkstra's algorithm		
#Exemplar/Case Studies: Compare passive localization (using RFID floor markers) vs. active localization (vision & LIDAR) in robots		
***Mapping of Course Outcomes**	**CO5**	
Learning Resources		

Text Books
T1. Robert J Schilling, Fundamentals of Robotics, Prentice Hall India, 200
Reference Books :
R1. John J Craig, Introduction to Robotics, Prentice Hall International, 2005
MOOC/NPTEL Courses links : ● **https://nptel.ac.in/courses/107106090**

24-HOC-ET-2-02B: Fundamental of Power Electronics

Teaching Scheme:	**Credits:** 3	**Examination Scheme:**
Theory: 3 Hours/Week		**CIE** : 20 Marks **MSE :** 20 Marks **SEE** : 60 Marks

Prerequisite Courses: 24-HOC-ET-2-01B Introduction to Robotics

Companion Course:

Course Objectives:

- Understand the role of power electronics in robotics.
- Analyze and design power electronic circuits for robotic systems.
- Study the integration of power electronic components with robotic actuators
- Explore applications like motor drives, battery management, and energy-efficient robotics.

Course Outcomes:
After completion of the course, learners should be able to

CONo	CO	BL
CO1	**Explain** power electronics devices and systems	**2**
CO2	**Apply** the principles of power conversion to optimize energy utilization and performance	**3**
CO3	**Design** magnetic devices for energy storage and conversion	**5**
CO4	**Explain** Drive Circuits and Control	**2**

Course Contents

Unit I	**Semiconductor Devices**	**7 Hours**

Ideal switch, diode static characteristics, diode dynamic characteristics, reading the diode datasheet, thermal dissipation, heatsink design, DIAC and TRIAC, Bipolar junction transistor - operation, static and dynamic characteristics, loss calculation, safe operation area, reading the datasheet, parallel operation, darlington connection

#Exemplar/Case Studies: Analyze how real switches (MOSFETs, IGBTs) deviate from ideal switch behavior in practical circuits

***Mapping of Course Outcomes**	**CO1**

Unit II	**MOSFETs IGBTs and Rectifiers**	**7 Hours**

MOSFETs and IGBTs - Operation, static and dynamic characteristics of MOSFET and IGBT, parallel operation, loss calculation and simulation. Rectifier - Capacitor filter, circuit operation and waveforms, designing the circuit, setting up for simulation in ngSpice, simulation of circuit, Inrush current limiting in rectifier-capacitor filter circuits, resistor solution, thermistor solution,

transformer solution, MOSFET solution, relay and contactor solution, power factor concepts and measurement of power factor for rectifier capacitor filter circuit.		
#Exemplar/Case Studies: Explore the design and operation of a rectifier with a capacitor filter, including circuit waveforms, component selection, and setting up simulations in ngSpice		
***Mapping of Course Outcomes**	**CO1**	
Unit III	**Converters**	**7 Hours**
Linear DC -DC converter or linear regulators, shunt regulator, operation, design and applications, series regulator, operation and design, improvement solutions, datasheet study, DC-DC switched mode converters : Buck, Boost and buck-boost converters, operation, waveforms, equations and simulation in ngSpice		
#Exemplar/Case Studies: Examine the role of shunt regulators in managing voltage levels in EV battery packs		
***Mapping of Course Outcomes**	**CO2**	
Unit IV	**Forward converter**	**7 Hours**
Forward converter operation, waveforms, core resetting methods, simulation in ngSpice, Inductor design by area product approach, Flyback converter, operation and waveforms.		
#Exemplar/Case Studies: Examine the Flyback Converter used in low-power USB chargers for smartphones and tablets		
***Mapping of Course Outcomes**	**CO2**	
Unit V	**Magnetics design**	**7 Hours**
Magnetics design, permeance, inductor value and energy storage, inductor design, transformer design area product approach		
#Exemplar/Case Studies: Design of a high-frequency transformer for an offline SMPS (Switched-Mode Power Supply)		
***Mapping of Course Outcomes**	**CO3**	
Unit VI	**Drive Circuits and Control**	**7 Hours**
Push pull, half bridge and full bridge circuits, operation and waveforms, simulation example, Drive circuits, BJT drive requirements, drive circuit non-isolated, drive circuits isolated, MOSFET drive requirements, drive circuit non-isolated and isolated, series snubber, shunt snubber, Close loop control, current control, slope compensation for current control, single phase inverter with sinusoidal PWM, simulation example		
#Exemplar/Case Studies: Study the design, operation, and waveform analysis of push-pull, half-bridge, and full-bridge converters used in high-power DC-DC conversion.		
***Mapping of Course Outcomes**	**CO4**	
Learning Resources		

Text Books
T1. Modern Robotics: Mechanics, Planning, and Control by Kevin M. Lynch and Frank C. Park **T2**. Power Electronics by P.S. Bimbhra **T3.** Power Electronics: Devices, Circuits, and Applications by M.D. Singh and K.B. Khanchandani **T4.** Battery Management Systems: Design by Simulation and Applications by K. S. Rajasekaran
Reference Books :
R1. Power Electronics by Muhammad H. Rashid
MOOC/NPTEL Courses links : ● **https://nptel.ac.in/courses/108101126**

Mid Semester Examination (MSE: March 2025)

Programme: AIDS/Civil/Computer/E&TC/Mechanical/MBA-I	
Class	**Pattern:**
Course Name:	**Course Code:**
AY:	**Semester:**
Time:	**Maximum Marks:** 20

Instructions to the candidates:

1. *Solve Q.1 OR Q.2, Q.3 OR Q.4, Q.5 OR Q.6*
2. *Bold-faced figures to the right indicate full marks.*
3. *Assume the suitable data if necessary*
4. *Any other instruction required for particular course may be added by subject/course chairman*

QN	Question	Mark
1a)	Q 1 can be bifurcated to maximum two sub questions	07
1b)		
	OR	
2	Q 2 can be bifurcated to maximum two sub questions	07
3	Q 3 can be bifurcated to maximum two sub questions	07
	OR	
4	Q 4 can be bifurcated to maximum two sub questions	07
5	Q 5 can be bifurcated to maximum two sub questions	06
	OR	
6	Q 6 can be bifurcated to maximum two sub questions	06

Shree Neminath Jain Brahmacharyashram's
Late Sau. Kantabai Bhavarlalji Jain College of Engineering
Neminagar, Chandwad -423 101 Dist. Nashik.
An Autonomous Institute, Affiliated to Savitribai Phule Pune University, Pune

Semester End Examination (Regular) <<Month Year>>

Programme: Class:

Course and Code: Semester

Academic Year: Pattern:

Time: 2Hr 30 Min Examination: SEE (Month Year) Max. Marks: 60

Instructions to the candidates:

1. *Solve Q.1 OR Q.2, Q.3 OR Q.4, Q.5 OR Q.6, Q.7 OR Q.8*
2. *Bold-faced figures to the right indicate full marks.*
3. *Assume the suitable data if necessary, but Justify it.*
4. *Draw the neat labelled diagrams, wherever necessary.*

QN	Question	Marks
1 a)	Unit I	6
1 b)	Unit II	7
1 c)	Unit III	7
	OR	
2 a)	Unit I	6
2 b)	Unit II	7
2 c)	Unit III	7
3 a)	Unit IV	7
3 b)	Unit IV	7
	OR	
4 a)	Unit IV	7
4 b)	Unit IV	7
5 a)	Unit V	7
5 b)	Unit V	6
	OR	
6 a)	Unit V	7
6 b)	Unit V	6
7 a)	Unit VI	7
7 b)	Unit VI	6
	OR	
8 a)	Unit VI	7
8 b)	Unit VI	6

Supporting Document

Sr. No.	Syllabus Contains	Short Answer	Yes / No	Page No. (In Syllabus)
1	अभ्यासक्रम	Enclosed in Syllabus	Yes	1
2	पात्रता	(As per the Rules and Regulations mentioned in MoM)	Yes	23
3	अभ्यासक्रमाची उद्दिष्टे	Enclosed in Syllabus	Yes	9
4	विषयाचे नाव	Enclosed in Syllabus	Yes	6
5	घटकांचा तपशील	Enclosed in Syllabus	Yes	6
6	तासिका	Enclosed in Syllabus	Yes	6
7	श्रेयांक पद्धत	Enclosed in Syllabus	Yes	6
8	संदर्भ साहित्य	Enclosed in Syllabus	Yes	10
9	संदर्भ ग्रंथ	Enclosed in Syllabus	Yes	10
10	प्रश्नपत्रिकेचे स्वरूप	Enclosed in Syllabus	Yes	21
11	अंतर्गत मूल्यमापनाचे स्वरूप	Enclosed in Syllabus	Yes	6
12	सत्र परीक्षेचे स्वरूप	Enclosed in Syllabus	Yes	22
13	गुणांकन	Enclosed in Syllabus	Yes	6