



SNJB'S Late Sau K B Jain College of Engineering, Chandwad
Department of Electronics & Telecommunication Engineering

Academic Year: 2023-24	Class: BE
Semester: I	Date: 4 /9 /2023

Title of Innovation method/activity: Crossword Puzzle

Name of Faculty: Prof. Agrawal R K

Subject: VLSI Design

Objective: To clarify the basic concepts related to the topic.

Topic Covered through Activity: VHDL Basic, PLD Architecture

Benefits: Enhanced understanding, improves engagement, stimulates thinking capacity and boosts confidence.

The method:

- Topic wise answer and clue pair is prepared on basic concepts.
- Crossword puzzle is prepared on online platform
<https://puzzlemaker.discoveryeducation.com/criss-cross> , <https://crosswordlabs.com/>
- Students are asked to submit the solved puzzle.

Activity Picture (Add picture of the activity if possible)

VHDL BASICS

ACROSS

1. CONCURRENT STATEMENT
3. MODELING STYLE
5. PIN DESCRIPTION

DOWN

2. SEQUENTIAL CIRCUIT
4. PLACE FOR COMMONLY USED FUNCTION

Use the clues to fill in the words above.
Words can go across or down.
Letters are shared when the words intersect.

5 of 6 words placed.

Unit 3: PLD Architecture

Across

2. Company manufacturing CPLD/FPGA
6. Advantage of CPLD/FPGA
9. Integrated circuit package type

Down

1. One time programming technique
3. Reprogramming technique
4. Programmable AND and fixed OR plane
5. Programmable AND and OR plane
7. Multiple PAL like blocks on single chip
8. Single chip having large number of logic blocks

Impact Analysis (Show the impact of the activity in examination)

- Questions were asked in the SPPU examination.

Total No. of Questions : 4] **SEAT No. :**

P5235 **[Total No. of Pages : 1**

[6188]-190
B.E. (E & TC) (Insem)
VLSI DESIGN AND TECHNOLOGY
(2019 Pattern) (Semester - VII) (Theory) (404182)

Time : 1 Hour] **[Max. Marks : 30**

Instructions to the candidates:

- 1) Attempt Q.1 or Q.2 and Q.3 or Q.4.
- 2) Draw neat diagram's wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.

Q1) a) Draw and explain design flow of VLSI. **[8]**
b) Write VHDL code for 8:1 mux using structural style of modeling. **[7]**

OR

Q2) a) Explain different modeling styles in VHDL. **[8]**
b) Write VHDL code for 4-bit ALU to perform different eight operations. **[7]**

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Spreadsheet shared with you | Criteria 5_Innovations in Teach... | Endsem VLSI - Google Drive | Innovation in TL-VLSI-22-23.doc |

drive.google.com/drive/u/0/folders/1gE7vTAQj96jcr6iGxI0Nl_YemVElZaf

Total No. of Questions : 8] SEAT No. :
P599 [6004]-548 [Total No. of Pages : 2

B.E. (Electronics & Telecommunication Engg.)
VLSI DESIGN & TECHNOLOGY
(2019 Pattern) (Semester - VII) (404182)

Time : 2½ Hours] [Max. Marks : 70

Instructions to the candidates:

- 1) Neat diagrams must be drawn wherever necessary.
- 2) Figures to the right indicate full marks.
- 3) Use of electronic pocket calculator is allowed.
- 4) Assume suitable data, if necessary.

Q1) a) Compare CPLD and FPGA on the basis of features, specifications and applications. [6]
b) Explain in brief classification of PLDs. [6]
c) Explain various stages of Synthesis in FPGA with suitable diagram. [6]

OR

Q2) a) Draw and explain the architecture of FPGA. Explain CLB in detail. [10]
b) Explain Clock Management Techniques in FPGA. [8]

Q3) a) Design CMOS logic for $Y = AB + CD$. Calculate W/L ratio for NMOS and PMOS area needed on chip. Find the total area. [9]
b) Discuss need for transmission gate. Draw 4 : 1 Mux using TG. [8]

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