ESTD - 1928

SNJB

SNJB'S Late Sau K B Jain College of Engineering, Chandwad
Department of Electronics & Telecommunication Engineering

Academic Year: 2022-23	Class: BE
Semester: I	Date: 15 /9/2022

Title of Innovation method/activity: Crossword Puzzle

Name of Faculty: Prof. Agrawal R K

Subject: VLSI Design

Objective: To clarify the basic concepts related to the topic.

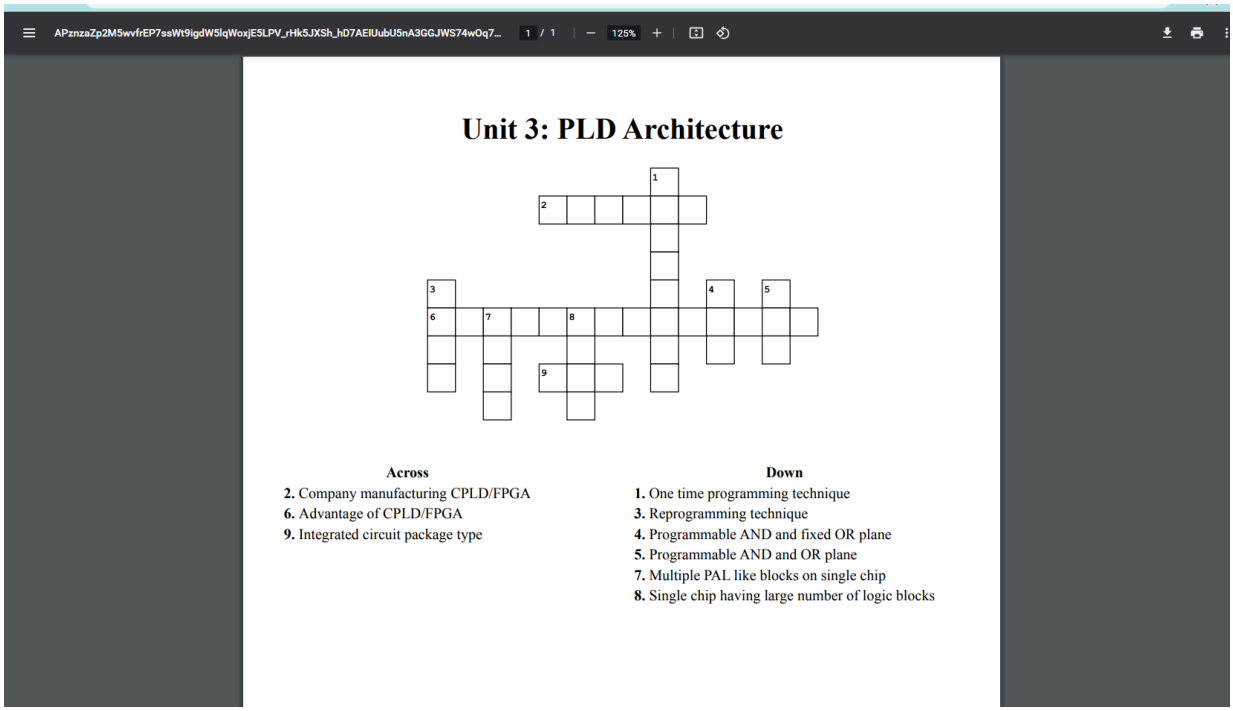
Topic Covered through Activity: VHDL Basic, PLD Architecture

Benefits: Enhanced understanding, improves engagement, stimulates thinking capacity and boosts confidence.

The method:

- Topic wise answer and clue pair is prepared on basic concepts.
- Crossword puzzle is prepared on online platform **https://puzzlemaker.discoveryeducation.com/criss-cross** , **https://crosswordlabs.com/**
- Students are asked to submit the solved puzzle.

Activity Picture (Add picture of the activity if possible)



Impact Analysis (Show the impact of the activity in examination)

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B.E. (E & T ... nester - VII)

VLSI DESIGN AND TECHNOLOGY

(2019 Pattern) (404182)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) *Attempt Q. No. 1 or Q. No. 2 and Q. No. 3 or Q. No. 4.*
2) *Neat diagrams must be drawn wherever necessary.*
3) *Figures to the right indicate full marks.*
4) *Assume suitable data, if necessary.*

Q1) a) What is meant by concurrent and sequential statements in VHDL? Describe with two examples of each. **[5]**

b) What is meant by synthesizable and non-synthesizable statement? Give two example of each. **[5]**

c) Write VHDL code for 4:1 Mux using behavioral modeling style. **[5]**

OR

Q2) a) Write VHDL Code for full adder and its test bench. **[10]**

b) Explain in brief different modeling styles supported by VHDL. **[5]**

Q3) a) What is Clock Skew? What are techniques to minimize it? **[5]**

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B.E. (Electronics & Telecommunication Engineering)

VLSI DESIGN & TECHNOLOGY

(2019 Pattern) (Semester - VII) (404182)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates :

1) *Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.*
2) *Neat diagrams must be drawn wherever necessary.*
3) *Figures to the right indicate full marks.*
4) *Use of electronic pocket calculator is allowed.*
5) *Assume sitable data, if necessary.*

Q1) a) Draw and explain the architecture of CPLD. Explain Macrocell in detail. **[10]**

b) What are the technologies supported by FPGA? Explain any two of it detail. **[8]**

OR

Q2) a) List and Explain in brief various Simulation and Synthesis Tool. **[6]**

b) Draw and Explain the following for FPGA : **[12]**

i) Logic Cell

ii) Programmable Switch Matrix

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- Questions were asked in the SPPU examination.

For review and critique contact: e-mail address of faculty and HOD

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Module Coordinator

HoD & Subject Incharge
Prof. Dr. Agrawal R K