



SNJB

**SNJB'S Late Sau K B Jain College of Engineering, Chandwad
Department of Electronics & Telecommunication Engineering**

Academic Year: 2022-23	Class: BE
Semester: I	Date: 29/10/2022

Title of Innovation method/activity: Virtual Lab.

Name of Faculty: Prof. Mechkul M. A.

Subject: PLC SCADA and Automation

Objective: To implement logic on PLC virtual lab.

Topic Covered through Activity:

1. Implementation Of PLC Arithmetic Instructions
2. Study of PID controller instruction for a pilot plant

Benefits: Virtual Lab concept to implement said logic in PLC program

The method:

- Students can access virtual lab through following links:
 1. <http://plc-coep.vlabs.ac.in/exp7/Theory.html?domain=Electrical%20Engineering&lab=Welcome%20to%20Programmable%20Logic%20Controller%20Lab>.
 2. <http://plc-coep.vlabs.ac.in/exp8/Aim.html?domain=Electrical%20Engineering&lab=Programmable%20Logic%20Controller%20Lab>
- As per procedure given in virtual lab, students prepare the ladder diagram
- Students observe the result through simulation.

Assessment Tools & Rubrics:

- As per practical rubrics.

Evaluation Sheet:

Department of Electronics and Telecommunication Engineering
Subject: Lab Practice 1 (Elective III: PLC, SCADA and Automation) (404184)
Experiment No. V1
Title: Implementation Of PLC Arithmetic Instructions (Virtual Lab)

Name of Student: _____
Date of Completion: _____ Date of Submission: _____

S.N.	Criteria	Obtained Marks
1	Answers (25%)	
2	Viva (25%)	
3	Programming Efficiency (25%)	
4	Timely Completion(25%)	
	Total	

Date: _____ Prof. Mechkul M. A.
(Subject Teacher)

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Impact Analysis (Show the impact of the activity in examination)

docs.google.com/spreadsheets/d/17inwsaNSiKKGu4P53Eic71tskdufIBAsf_3E8WKsNjc/edit#gid=1181461077

CO Attainment VLSI_PSA_Lab_2022-23

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100% 123 Camb... - 11 + B I A

A1:BL1 SNJB's Late Sau. KBJ College of Engineering, Chandwad.

1
2
3 Academic Year: 2022-23 Batch:B1 and B2
4 of Staff: Mechkul M. A.
5 Rubrics
6
7
8
9

#	E6					E7					E8					E9					V1					V2													
	R5	Total	R1	R2	R3	R4	R5	Total	R1	R2	R3	R4	R5	Total	R1	R2	R3	R4	R5	Total	R1	R2	R3	R4	R5	Total	R1	R2	R3	R4	R5	Total							
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CO VLSI_Rubrics VLSI_TW PSA_Rubrics PSA_TW Final Termwork Marks CO Analysis_Direct VLSI

https://docs.google.com/spreadsheets/d/17inwsaNSiKKGu4P53Eic71tskdufIBAsf_3E8WKsNjc/edit#gid=1181461077

Activity Picture (Add picture of the activity if possible)

plc-coep.vlabs.ac.in/exp/implementation-logic-gates/simulation.html

Implementation of Logic Gates

Programmable Logic Controller

Open Save Compile Run Development

innovation in TL...docx Show all

For review and critique contact: e-mail address of faculty and HOD

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Subject In charge

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