ESTD - 1928

SNJB

SNJB'S Late Sau K B Jain College of Engineering, Chandwad
Department of Electronics & Telecommunication Engineering

Academic Year: 2023-24	Class: BE
Semester: I	Date:27/9/2023

Title of Innovation method/activity: Flipped classroom

Name of Faculty: Prof. Agrawal R K

Subject: VLSI Design

Objective: To write HDL code in Verilog

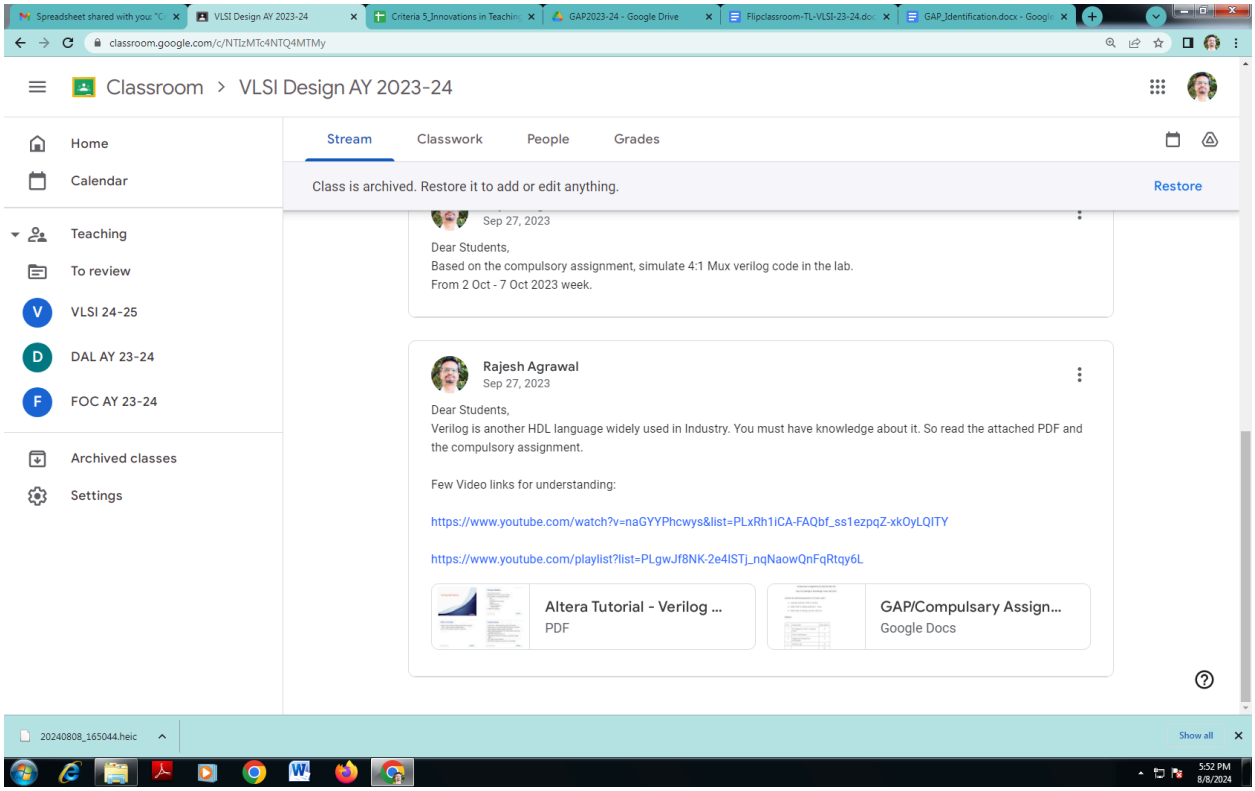
Topic Covered through Activity: Verilog Language

Benefits: Able to differentiate between VHDL & Verilog language and write Verilog code for Digital systems.

The method:

- Study material is shared on Google classroom.
- Students presented the topic in the classroom.
- Students are asked to submit the assignment.

Activity Picture (Add picture of the activity if possible)



Impact Analysis (Show the impact of the activity in examination)

Students have solved the given assignment on Verilog code.

For review and critique contact: e-mail address of faculty and HOD

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Module Coordinator

HoD & Subject Incharge
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